

CLAIM AMENDMENTS:

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided below. Notably, the status of each claim is indicated in the parenthetical expression adjacent to the corresponding claim number.

Claims 1 - 27 (**Canceled**).

- 1 28. **(Currently Amended)**: A semiconductor memory array comprising:
 - 2 a plurality of memory cells arranged in a matrix of rows and columns, the plurality
 - 3 of memory cells include a first memory cell and a second memory cell, wherein the first
 - 4 and second memory cells each include at least a transistor to constitute the memory cell
 - 5 and wherein the transistor includes:
 - 6 a source region;
 - 7 a drain region;
 - 8 a body region disposed between ~~and adjacent to~~ the source region and
 - 9 the drain region, wherein the body region is electrically floating; and
 - 10 a gate spaced apart from, and capacitively coupled to, the body region;
 - 11 wherein each memory cell includes:
 - 12 a first data state representative of a first charge in the body region; and
 - 13 a second data state representative of a second charge in the body region
 - 14 wherein the second charge is substantially provided by removing charge
 - 15 from the body region through the source region; and
 - 16 wherein the drain region of the transistor of the first memory cell and the drain
 - 17 region of the transistor of the second memory cell are the same region.

1 29. (Currently Amended): The memory array of claim 28 wherein the plurality
2 of memory cells further includes a third memory cell wherein the third memory cell
3 includes at least a transistor to constitute the memory cell and wherein the transistor
4 includes:
5 a source region;
6 a drain region;
7 a body region disposed between ~~and adjacent to~~ the source region and
8 the drain region, wherein the body region is electrically floating; and
9 a gate spaced apart from, and capacitively coupled to, the body region;
10 wherein each memory cell includes:
11 a first data state representative of a first charge in the body region; and
12 a second data state representative of a second charge in the body region
13 wherein the second charge is substantially provided by removing charge
14 from the body region through the source region; and
15 wherein the source region of the transistor of the second memory cell and the
16 source region of the transistor of the third memory cell are the same region.

1 30. (Currently Amended): The memory array of claim 28 further including a
2 control unit, coupled to the gate and the drain region of the transistor of the first memory
3 cell, to provide control signals to the transistor of the first memory cell, wherein the
4 transistor of the first memory cell, in response to a first write control signals signal set,
5 stores the first charge in the body region and wherein the first charge is comprised of an
6 accumulation of majority carriers in the body region.

1 31. **(Currently Amended)**: The memory array of claim 30 wherein the majority
2 carriers accumulate in a portion of the body region that is adjacent to the source region
3 of the transistor of the first memory cell and wherein the source regions of the
4 transistors of the first and second memory cell are connected to a fixed voltage.

1 32. **(Currently Amended)**: The memory array of claim 28 further including a
2 control unit, coupled to the gate and the drain region of the transistor of the first memory
3 cell, to provide control signals to the transistor of the first memory cell, wherein the
4 transistor of the first memory cell, in response to a second write control signals signal
5 set, stores the second charge in the body region wherein the second charge is
6 substantially provided by removing charge from the body region through the source
7 region.

1 33. **(Currently Amended)**: The memory array of claim 32 wherein the second
2 write control signals include signal set includes at least first and second signals having
3 positive voltages wherein the first signal is applied to the drain region of the transistor of
4 the first memory cell and the second signal is applied to the gate of the transistor of the
5 first memory cell.

1 34. **(Currently Amended)**: The memory array of claim 28 further including:
2 a reading unit, coupled to the drain region of the transistor of the first memory
3 cell, to determine the data state of the first memory cell;

4 a control unit, coupled to gate of the transistor of the first memory cell, to provide
5 control signals to the transistor of the first memory cell; and
6 wherein, in response to a read control signal applied to the gate of the transistor
7 of the first memory cell by the control unit, the reading unit determines the charge stored
8 in the body region of the transistor of the first memory cell.

1 35. (Currently Amended): A semiconductor memory array comprising:
2 a plurality of memory cells arranged in a matrix of rows and columns, the plurality
3 of memory cell include a first memory cell and a second memory cell, wherein the first
4 and second memory cells each include at least a transistor to constitute the memory cell
5 and wherein the transistor includes:
6 a source region having impurities to provide a first conductivity type;
7 a drain region having impurities to provide the first conductivity type,
8 a body region disposed between ~~and adjacent to~~ the source region and
9 the drain region wherein the body region is electrically floating and includes
10 impurities to provide a second conductivity type wherein the second conductivity
11 type is different than the first conductivity type;
12 a gate disposed over the body region;
13 wherein the memory cell includes:
14 a first data state representative of a first charge in the body region wherein
15 the first charge is substantially provided by impact ionization; and
16 a second data state representative of a second charge in the body region
17 wherein the second charge is substantially provided by removing charge from the
18 body region through the source region; and

19 wherein the drain region of the transistor of the first memory cell and the drain
20 region of the transistor of the second memory cell are the same region.

1 36. **(Currently Amended)**: The memory array of claim 35 wherein the plurality
2 of memory cells further includes a third memory cell wherein the third memory cell
3 includes at least a transistor to constitute the memory cell and wherein the transistor
4 includes:

5 a source region having impurities to provide a the first conductivity type;
6 a drain region having impurities to provide the first conductivity type,
7 a body region disposed between ~~and adjacent to~~ the source region and
8 the drain region wherein the body region is electrically floating and includes
9 impurities to provide the a second conductivity type ~~wherein the second~~
10 ~~conductivity type is different than the first conductivity type;~~

11 a gate disposed over the body region;

12 wherein the memory cell includes:

13 a first data state representative of a first charge in the body region wherein
14 the first charge is substantially provided by impact ionization; and

15 a second data state representative of a second charge in the body region
16 wherein the second charge is substantially provided by removing charge from the
17 body region through the source region; and

18 wherein the source region of the transistor of the second memory cell and the
19 source region of the transistor of the third memory cell are the same region.

1 37. (Currently Amended): The memory array of claim 35 further including a
2 control unit, coupled to the gate and drain region of the transistor of the first memory
3 cell, to apply control signals to the transistor of the first memory cell wherein the control
4 signals include a first write control signals signal set to accumulate the first charge in the
5 body of the transistor of the first memory cell and a second write control signals signal
6 set to provide the second charge in the body region of the transistor of the first memory
7 cell by removing charge from the body region through the source region of the transistor
8 of the first memory cell.

1 38. (Currently Amended): The memory array of claim 37 wherein the first write
2 control signals include charge is stored in the body region of the first memory cell in
3 response to applying a first signal, having a first negative voltage, applied to the drain
4 region of the transistor of the first memory cell and a second signal, having a second
5 negative voltage, applied to the gate of the transistor of the first memory cell.

1 39. (Currently Amended): The memory array of claim 38 wherein the transistor
2 of the first memory cell stores at least a substantial portion of the first charge in a
3 portion of the body region of the transistor of the first memory cell that is adjacent to the
4 source region of the transistor of the first memory cell.

1 40. (Currently Amended): The memory array of claim 37 wherein the second
2 write control signals include signal set includes a first signal, having a first positive
3 voltage, applied to the drain region of the transistor of the first memory cell and a

4 second signal, having a second positive voltage, applied to the gate of the transistor of
5 the first memory cell.

1 41. **(Currently Amended)**: The memory array of claim 40 wherein the source
2 regions of the transistors of the first and second memory cells are connected to a fixed
3 voltage.

1 42. **(Currently Amended)**: The memory array of claim 41 40 wherein the
2 second charge is stored in the body region of the transistor of the first memory cell in
3 response to removing the first positive voltage from the drain region of the transistor of
4 the first memory cell before removing the second positive voltage from the gate of the
5 transistor of the first memory cell.

1 43. **(Currently Amended)**: The memory array of claim 42 40 wherein, in
2 response to the first and second positive voltages, the transistor of the first memory cell
3 includes a forward bias current between its body region and its source region.

1 44. **(Currently Amended)**: The memory array of claim 43 wherein the second
2 charge is stored in the body region of the transistor of the first memory cell in response
3 to removing the first positive voltage from the drain region of the transistor of the first
4 memory cell and the second positive voltage from the gate of the transistor of the first
5 memory cell.

1 45. (Currently Amended): The memory array of claim 35 further including:
2 a reading unit, coupled to the drain region of the transistor of the first memory
3 cell, to determine the data state of the first memory cell;
4 a control unit, coupled to gate of the transistor of the first memory cell, to provide
5 control signals to the transistor of the first memory cell; and
6 wherein, in response to a read control signal applied to the gate of the transistor
7 of the first memory cell by the control unit, the reading unit senses the charge stored in
8 the body region of the transistor of the first memory cell.

1 46. (Currently Amended): The memory array of claim 37 35 further including a
2 control unit, coupled to the gate and drain region of the transistor of the first memory
3 cell, to apply control signals to the transistor of the first memory cell wherein the control
4 signals include first write control signals to accumulate the first charge in the body of the
5 transistor of the first memory cell and second write control signals to provide the second
6 charge in the body region of the transistor of the first memory cell by removing charge
7 from the body region through the source region of the transistor of the first memory cell;
8 and
9 wherein the second write control signals include signal set includes a first signal,
10 having a first positive voltage, applied to the drain region of the transistor of the first
11 memory cell.

1 47. (Currently Amended): The memory array of claim 46 wherein the second
2 write control signals include a second signal, having a second positive voltage, applied
3 to the gate of the transistor of the first memory cell and wherein the second charge is

4 stored in the body region of the transistor of the first memory cell in response to
5 removing the first positive voltage from the drain region of the transistor of the first
6 memory cell before removing the second positive voltage from the gate of the transistor
7 of the first memory cell.

1 **48. (Currently Amended):** The memory array of claim 47 wherein, in response
2 to the first and second positive voltages, the transistor of the first memory cell includes a
3 forward bias current between its body region and its source region.

1 **49. (Currently Amended):** The memory array of claim 48 wherein the second
2 charge is stored in the body region of the transistor of the first memory cell in response
3 to removing the first positive voltage from the drain region of the transistor of the first
4 memory cell and wherein the source regions of the transistors of the first and second
5 memory cells are connected to a fixed voltage.

1 **50. (Currently Amended):** A semiconductor memory array, disposed in or on a
2 semiconductor region or layer which resides on or above an insulating region or layer of
3 a substrate, the semiconductor memory array comprising:
4 a plurality of memory cells, including a first memory cell and a second memory
5 cell, arranged in a matrix of rows and columns and disposed in or on the semiconductor
6 region or layer, including a first memory cell and a second memory cell, wherein the first
7 and second memory cells each include at least a transistor to constitute the memory cell
8 and wherein the transistor includes:

9 a source region having impurities to provide a first conductivity type;
10 a drain region having impurities to provide the first conductivity type,
11 a body region disposed between ~~and adjacent to~~ the source region, ~~and~~
12 the drain region and the insulating region or layer of the substrate, wherein the
13 body region is electrically floating and includes impurities to provide a second
14 conductivity type wherein the second conductivity type is different than the first
15 conductivity type;
16 a gate spaced apart from, and capacitively coupled to, the body region,
17 wherein the memory cell includes:
18 a first data state representative of a first charge in the body; and
19 a second data state representative of a second charge in the body region
20 wherein the second charge is substantially provided by removing charge from the
21 body region through the source region; and
22 wherein the drain region of the transistor of the first memory cell and the drain
23 region of the transistor of the second memory cell are the same region.

1 51. **(Currently Amended):** The memory array of claim 50 wherein the plurality
2 of memory cells further includes a third memory cell wherein the third memory cell
3 includes at least a transistor to constitute the memory cell and wherein the transistor
4 includes:
5 a source region having impurities to provide a the first conductivity type;
6 a drain region having impurities to provide the first conductivity type,
7 a body region disposed between ~~and adjacent to~~ the source region, ~~and~~ the drain
8 region and the insulating region or layer of the substrate, wherein the body region is

9 electrically floating and includes impurities to provide the a second conductivity type
10 wherein the second conductivity type is different than the first conductivity type;
11 a gate spaced apart from, and capacitively coupled to, the body region;
12 wherein the memory cell includes:
13 a first data state representative of a first charge in the body; and
14 a second data state representative of a second charge in the body region wherein
15 the second charge is substantially provided by removing charge from the body
16 region through the source region; and
17 wherein the source region of the transistor of the second memory cell and the
18 source region of the transistor of the third memory cell are the same region.

1 **52. (Currently Amended):** The memory array of claim 50 further including a
2 control unit, coupled to the transistor of the first memory cell, to control the data state of
3 the first memory cell wherein, in response to a first voltage applied to the drain region of
4 the transistor of the first memory cell and a second voltage applied to the gate of the
5 transistor of the first memory cell, the first charge is removed from the body region of
6 the transistor of the first memory cell through its source region.

1 **53. (Currently Amended):** The memory array of claim 52 wherein the control
2 unit, in response to removing the first voltage from the drain region of the transistor of
3 the first memory cell before removing the second voltage from the gate of the transistor
4 of the first memory cell, causes the second charge to be stored in the body region of the
5 transistor of the first memory cell.

1 54. **(Currently Amended)**: The memory array of claim 52 wherein the control
2 unit, in response to applying ground to the drain region of the transistor of the first
3 memory cell before removing the second voltage from the gate of the transistor of the
4 first memory cell, causes the second charge to be stored in the body region of the
5 transistor of the first memory cell.

1 55. **(Currently Amended)**: The memory array of claim 52 wherein the control
2 unit, in response to applying a third voltage to the drain region of the transistor of the
3 first memory cell before applying a fourth voltage to the gate of the transistor of the first
4 memory cell, causes the transistor of the first memory cell to store the second charge in
5 its body region.

1 56. **(Currently Amended)**: The memory array of claim 52 wherein the transistor
2 of the first memory cell stores the first charge in a portion of its body region that is
3 adjacent to its source region.

1 57. **(Currently Amended)**: The memory array of claim 52 50 further including a
2 control unit, coupled to the gate and the drain region of the transistor of the first memory
3 cell, to apply control signals to the transistor of the first memory cell wherein:
4 in response to a first write control signals signal-set, the transistor of the first
5 memory cell generates and stores the first charge in the body region; and
6 in response to a second write control signals signal-set, the transistor of the first
7 memory cell generates and stores the second charge in the body region wherein the

8 transistor of the first memory cell generates the second charge by removing charge
9 from its body region through its source region; and

10 wherein the first and second write control signals ~~signal sets~~ each include a
11 plurality of signals.

1 58. (Currently Amended): The memory array of claim 57 wherein the first write
2 control signals ~~signal set includes~~ a first signal, having a first negative voltage
3 applied to the drain ~~of the transistor of the first memory cell~~, and a second signal, having
4 a second negative voltage applied to the gate ~~of the transistor of the first memory cell~~,
5 and wherein, in response to removing the first and second negative voltages, the first
6 charge is stored in the body region ~~of the transistor~~ of the first memory cell.

1 59. (Currently Amended): The memory array of claim 57 wherein the transistor
2 of the first memory cell stores the first charge in a portion of the body region of the
3 transistor of the first memory cell that is adjacent to the source region of the transistor of
4 the first memory cell.

1 60. (Currently Amended): The memory array of claim 57 wherein the second
2 write control signals ~~signal set includes~~ a first signal having a first positive
3 voltage applied to the drain region and a second signal having a second positive voltage
4 applied to the gate.

1 61. **(Currently Amended)**: The memory array of claim 60 wherein the second
2 charge is stored in the body region of the transistor of the first memory cell in response
3 to removing the first positive voltage from the drain region of the transistor of the first
4 memory cell before removing the second positive voltage from the gate of the transistor
5 of the first memory cell.

1 62. **(Currently Amended)**: The memory array of claim 61 wherein, in response
2 to the first and second positive voltages, the transistor of the first memory cell includes a
3 forward bias current between its body region and the source region.

1 63. **(Currently Amended)**: The memory array of claim 62 60 wherein the
2 second charge is stored in the body region of the transistor of the first memory cell in
3 response to removing the first positive voltage from the drain region of the transistor of
4 the first memory cell and the second positive voltage from the gate of the transistor of
5 the first memory cell.

1 64. **(Currently Amended)**: The memory array of claim 50 further including:
2 a reading unit, coupled to the drain region of the transistor of the first memory
3 cell, to determine the data state of the first memory cell;
4 a control unit, coupled to gate of the transistor of the first memory cell, to provide
5 control signals to the transistor of the first memory cell; and

6 wherein, in response to a read control signal applied to the gate of the transistor
7 of the first memory cell by the control unit, the reading unit senses the charge stored in
8 the body region of the transistor of the first memory cell.